CLAIMS

I claim:

1. An apparatus for distributing synchronized clock signals to multiple sites, the apparatus comprising:

a clock input configured as a solder bump;

a first driver coupled to said clock input; and

a first receiver coupled to said driver.

2. The apparatus for distributing synchronized clock signals to multiple sites of claim 1, further comprising a first transmission line spanning between said first driver and said first receiver.

3. The apparatus for distributing synchronized clock signals to multiple sites of claim 2, further comprising a second driver, a second receiver, and a second transmission line.

4. The apparatus for distributing synchronized clock signals to multiple sites of claim 3, wherein said first transmission line and said second transmission line comprise substantially equal time delay.

5. The apparatus for distributing synchronized clock signals to multiple sites of claim 1, further comprising multiple transmission lines spanning between said first receiver and said second receiver.

6. The apparatus for distributing synchronized clock signals to multiple sites of claim 5, wherein at least two of said plurality of transmission lines are configured to cancel noise.

7. The apparatus for distributing synchronized clock signals to multiple sites of

claim 1, an output configured as a bump.

8. The apparatus for distributing synchronized clock signals to multiple sites of claim 1, wherein the apparatus is formed using SiGe.

9. A microelectronic device configured to supply synchronic clock signals to a microprocessor, said microelectronic device comprising:

an input;

a clock driver coupled to said input;

a transmission line coupled to said clock driver;

a receiver coupled to said transmission line; and

an output coupled to said receiver.

10. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 9, further comprising a plurality of outputs.

11. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 9, further comprising a plurality of drivers and a plurality of receivers.

12. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 9, wherein said input is configured as a solder bump.

13. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 9, wherein said output is configured as a solder bump.

14. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 9, wherein said transmission line is shielded.

15. The microelectronic device configured to supply synchronic clock signals to a

microprocessor of claim 9, further comprising a second transmission line coupled to a second driver and a second receiver.

16. The microelectronic device configured to supply synchronic clock signals to a microprocessor of claim 15, wherein said second transmission line exhibits about the same delay as said transmission line.